REMARKS

Claims 1-25 remain in this application. The Office Action has indicated that claims 2-6, 11-18 and 20-25 are allowed.

REJECTIONS TO THE CLAIMS UNDER 35 U.S.C. § 103(a)

Claims 1, 7-10, and 19 were rejected under 35 U.S.C. § 102(b) as being anticipated U.S. Patent No. 5,034,744 to Obinata ("Obinata"). Claims 8-9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Obinata.

As presented above, claim 1 recites "detecting a sample bit having one logic value and adjacent bits on both sides of said sample bit each having an opposite logic value to the one logic value of said sample bit" and "outputting the received word with the sample bit having said one logic value inverted." Independent claims 10 and 19 have similar limitations.

The newly cited Obinata reference does not teach or suggest these features. The current Office Action cites Col. 2, lines 46-62 and the Abstract of Obinata as support for teaching the detecting and outputting operations of claim 1. Col. 2, lines 48-55 states that "a detecting circuit" is provided "for detecting status changes that results in generation of glitches in digital data to be inputted into the DAC, a pulse generating circuit for generating deglitching pulses for suppressing the glitches in response to outputs of the detecting circuit, and an operation circuit for cancelling glitches included in converted outputs of the DAC." The language of the Abstract is similar.

Though Obinata discusses the detection of "status changes," Obinata does not teach or suggest detecting a sample bit having one logic value and adjacent bits on both sides of the sample bit having an opposite logic value. Looking at Fig. 1, serial data is provided by oversampling digital filter 20 to S/P converting circuit 23. Circuit 23 outputs 16-bit parallel values as bits O_1 to O_{16}. Values O_1 to O_4 are provided to D-type flip-flops 30-33. Looking at Fig. 1, and Col. 4, lines 47-57, it is clear that a comparison is made between a sample bit (i.e., the input into one of the D-type flip-flops) and the previous sample bit (i.e., the output of the same D-type flip-flop). Looking at D flip-flop 33, the comparison is made by XOR gate 37. If both inputs to this gate are the same, then the output will be a logic "0." If both inputs to this gate are different (indicating a glitch), then the output will be a logic "1" (or "H" as stated in Obinata). The outputs of the XOR gates 34-37 are used to make a correction of a particular type of glitch with the Philips TDA15431S1 DAC as explained in more detail at Col. 3, lines 14-45. The eventual outputs of NAND gates 46 and 47 are used in the analog circuits 27 and 28.

To summarize, though Obinata discusses the detection of "status changes," it is clear from the specification in Obinata, that such a "status change" is the situation where a previously sampled bit is different from a current sampled bit. There is no disclosure in Obinata, and the circuit of Fig. 1 does not support, detecting whether a sample bit has one logic value while adjacent **bits** on both sides of the sample bit have opposite logic values. Since there is no teaching or suggestion of this feature in Obinata, reconsideration and withdrawal of the rejection of claims 1, 10, and 19, as well as claims 7-9 (which depend from claim 1) under 35 U.S.C. §§ 102(b) and 103(a) is respectfully requested.

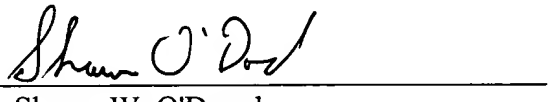
CONCLUSION

For all the above reasons, the Applicant respectfully submits that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (202) 220-4200 to discuss any matter concerning this application. The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. § 1.16 or § 1.17 to Deposit Account No. 11-0600.

Respectfully submitted,
KENYON & KENYON

Dated: May 15, 2006

By: 
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